Notice of References Cited	Application/Control No. 09/661,226	Applicant(s)/Patent Under Reexamination FAIRMAN ET AL.	
	Examiner Tam (Jenny) Phan	Art Unit 2144	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,613,114	03-1997	Anderson et al.	718/108
	B	US-6,519,265	02-2003	Liu et al.	370/463
	C	US-5,944,816	08-1999	Dutton et al.	712/215
	D	US-6,061,711	05-2000	Song et al.	718/108
	E	US-6,567,839	05-2003	Borkenhagen et al.	718/103
	F	US-6,651,163	11-2003	Kranich et al.	712/244
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
/	U	Kreuzinger, J.; Ungerer, T.; "Context-switching techniques for decoupled multithreaded processors" EUROMICRO Conference, 1999. Proceedings. 25th , Volume: 1 , 8-10 Sept. 1999 Pages:248 - 251 vol.1
/	V	Kekckler, S.W.; Chang, A.; Chatterjee, W.S.L.S.; Dally, W.J.; "Concurrent event handling through multithreading" Computers, IEEE Transactions on , Volume: 48 , Issue: 9 , Sept. 1999 Pages:903 - 916
/	W	Dean, A.G.; Shen, J.P.; "Techniques for software thread integration in real-time embedded systems" Real-Time Systems Symposium, 1998. Proceedings., The 19th IEEE , 2-4 Dec. 1998 Pages:322 - 333
	X	Fiske, S.; Dally, W.J.; "Thread prioritization: a thread scheduling mechanism for multiple-context parallel processors" High-Performance Computer Architecture, 1995. Proceedings. First IEEE Symposium on , 22-25 Jan. 1995 Pages:210 - 221

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.